of at least one of a plurality of configuration signals to arithmetic-logically configure the computing cell prior to processing the input signals, wherein coupled logic members perform at least one select arithmetic-logic operation on the input signals to process the input signals, the at least one select arithmetic-logic operation being dependent on the at least one of the plurality of configuration signals,

a register unit selectively storing a portion of the processed input signals, and

an output interface for transmitting the processed input signals,

wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells; and

a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to arithmetic-logically configure and arithmetic-logically reconfigure the at least some of the plurality of computing cells.

B1 Cmeld

35. (Amended) A massively parallel data processing apparatus, comprising:

a plurality of computing cells arranged in a multidimensional matrix, each of the plurality of computing cells being arithmetic-logically configurable and reconfigurable, each of the plurality of computing cells capable of processing a first plurality of data words simultaneously with the processing of a second plurality of data words by others of the plurality of computing cells, wherein each of the plurality of computing cells is arithmetic-logically configured by a first configuration signal to perform a first select arithmetic-logic operation, and wherein each of the plurality of computing cells is arithmetic-logically reconfigured to perform a second select

B2 Cmt

arithmetic-logic operation by a second configuration signal different than the first configuration signal, the first select operation being different than the second select operation; and

B2 Cncld

a plurality of buses, wherein each of the plurality of computing cells are connectable to at least one of the plurality of computing cells using at least one of the plurality of buses.

B3

43. (Amended) The massively parallel data processing apparatus of claim 42, further comprising:

a memory, coupled to the compiler, for storing the first configuration signal and the second configuration signal.

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47. (Amended) A massively parallel data processing apparatus, comprising:

B4 Cnt

a programmable logic device, the programmable logic device including a plurality of logic elements arranged in a multidimensional matrix, each of the plurality of logic elements being arithmetic-logically configurable and reconfigurable, each of the plurality of logic elements capable of processing a first plurality of binary signals simultaneously with the processing of a second plurality of binary signals by others of the plurality of logic units, wherein each of the plurality of logic elements is arithmetic-logically configured to perform a first select arithmetic-logic operation by a first configuration signal, and wherein each of the plurality of logic elements is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second configuration signal different than the first configuration signal, the first select operation being different than the second select operation, the programmable logic device further comprising a plurality of buses, wherein each of the plurality of logic elements are connectable to at least one of the plurality of logic elements using at least one

of the plurality of buses; and

at least one memory device coupled to the programmable logic device for storing at least one of i) multiple data to be processed by the programmable logic device, and ii) processing results of the programmable logic device.

B4 Cncld

53. (Amended) The massively parallel data processing apparatus of claim 52, further comprising:

a memory, coupled to the compiler, for storing the first configuration signal and the second configuration signal.

B5

69. (Amended) A method for configuring a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

grouping at least some of the cells into functional units;

processing data by the functional units; and

receiving, by a reconfiguration unit, state information regarding at least one of the functional units.

B6

72. (Amended) A method for configuring a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

individually configuring at least some of the cells to form functional units;

processing data by at least some of the functional units; and

receiving, by a reconfiguration unit, state information regarding at least one of the functional units; and

individually reconfiguring at least one cell of at least one of the functional units to form a different functional unit at a function of the state information, while simultaneously others of the functional units continue processing data.

B7 Cnt'd

73. (Amended) The method according to claim 72, further comprising the steps of:

transmitting, by the reconfiguration unit, reconfiguration data to the at least one cell, wherein the step of reconfiguring includes the step of reconfiguring, by the at least one cell, as a function of the reconfiguration data transmitted by the reconfiguration unit.

B7 Cncld

Please add the following new claims:

79. (New) The massively parallel data processing apparatus of claim 15, wherein the cell configuration memory is dedicated to storing configuration information.

80. (New) The massively parallel data processing apparatus of claim 47, further comprising:

at least one of i) an interface coupled to at least one external computer and ii) a further memory device coupled to the at least one external computer, for transferring at least one of multiple data to be processed by the programmable logic device and processing results of the programmable logic device.

B8 Cnt

81. (New) The method of configuring a data processor of claim 69, further comprising:

transmitting, by the reconfiguration unit, respective configuration data to the at least one of the functional units as a function of the received state information; and

reconfiguring at least one of the cells in the at least one of the functional units as a function of the respective configuration data while simultaneously other functional units continue processing data.

82. (New) The massively parallel data processing apparatus according to claim 15, wherein each of the computing cells includes a cell configuration memory adapted to store the at

least one of the plurality of configuration signals.

83. (New) The massively parallel data processing apparatus according to claim 17, wherein the selectively coupled computing cells together form a dataflow processor.

84. (New) The massively parallel data processing apparatus according to claim 35, wherein each of the computing cells includes a cell configuration memory adapted to store the first configuration signal and the second configuration signal.

B8 Cnt

85. (New) The massively parallel data processing apparatus according to claim 35, wherein each of the computing cells includes a plurality of logic members selectively coupled together in accordance with the first set of configuration words to arithmetic-logically configure the computing cell and in accordance with the second set of configuration words to arithmetic-logically reconfigure the computing cell.

86. (New) A massively parallel data processing apparatus comprising:

a plurality of computing cells arranged in a multidimensional matrix, the plurality of computing cells capable of simultaneously manipulating a plurality of data, each of the plurality of computing cells including:

an input interface for receiving a plurality of input signals,

a plurality of logic members, at least one of the plurality of logic members coupled to the input interface,

at least one coupling unit selectively coupling at least one of the plurality of logic members to another of the plurality of logic members a function of at least one of a plurality of configuration signals,

a cell configuration memory adapted to store

the at least one of the plurality of configuration signals,

a register unit selectively storing a portion of the processed input signals, and

an output interface for transmitting the processed input signals,

wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells; and

a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to arithmetic-logically configure and arithmetic-logically reconfigure the at least some of the plurality of computing cells.

B8 Cncl'd

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83. (New) The massively parallel data processing device according to claim 17, wherein the selectively coupled computing cells together form a dataflow processor.

REMARKS

Claim 15, 35, 43, 47, 53, 69, 72 and 73 have been amended to clarify the subject matter recited therein. New claims 79-83 have been added. Claims 15-83 are now pending. No new matter has been added. Reconsideration of the present application is requested.

Claims 15-34

Claims 15-31, 33 and 34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,794,059 to Barker et al. ("Barker"). Claim 32 stands rejected under 35 U.S.C. § 103 as being obvious over Barker in view of subject matter to which the Examiner has taken Official Notice. It is respectfully submitted that claims 15-31, 33 and 34 are not